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09/740,601	12/19/2000	Joe D. Bolding	10003151-1	3782

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EXAMINER
ROCHE, TRENTON J

ART UNIT	PAPER NUMBER
2124	4

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No.	Applicant(s)	
	09/740,601	BOLDING ET AL.	
	Examiner	Art Unit	
	Trent J Roche	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-25 have been examined.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In section b, it does not distinctly state which computer readable program code is performing the actions of part ii of the claim.

It is suggested that the wording of section b, part ii of claim 16 be changed to "code for selecting said one of said plurality of symbol tables."

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 4, 5, 7 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 4,769,770 to Miyadera et al.

Regarding claim 1:

Miyadera et al teach:

- selecting a symbol table ("the relocation tables are selected..." in col. 6 lines 42-43)
- providing a plurality of symbol tables ("a plurality of relocation tables may be provided." in col. 6 line 39)
- in a computer system ("information processing apparatus..." in col. 4 line 44)
- having an address pointer ("pointers are provided..." in col. 6 line 41)
- said symbol tables encompassing a range of addresses ("the upper/lower limit of the relocation range..." in col. 6 lines 30-31)
- identifying at least one of the plurality of symbol tables within whose range of addresses the address pointer is pointing ("the relocation tables are selected...by using the content of the pointer." in col. 6 lines 42-44)
- selecting at least one of the plurality of symbol tables ("the content corresponding to each job is written in each of the relocation tables...pointers are provided for identifying the relocation tables...the relocation tables are selected...by using the content of the pointer." in col. 6 lines 39-44. The tables are checked to see if the corresponding content is in a table, and if it is, the corresponding table is selected.)

Regarding claim 4:

The rejection of claim 1 is incorporated, and further, Miyadera et al inherently disclose a computer system performing the operations of claim 1. If a computer system were not present, no identifying or selecting would occur.

Regarding claim 5:

The rejection of claim 1 is incorporated, and further, Miyadera et al disclose a pointer to a memory location containing instructions to be executed ("the relocation tables are selected...by using the content of the pointer." in col. 6 lines 42-44. The content of the pointer would be the memory location of the relocation table.)

Regarding claim 7:

The rejection of claim 1 is incorporated, and further, Miyadera et al disclose a plurality of cells, each cell having a processing unit having at least one computer processor ("a plurality of processors performing addressing..." in col. 2 lines 44-45) further comprising identifying an active cell among the plurality of cells, wherein a symbol table is selected. Because a relocation table is selected as noted in the rejection of claim 1, then there is inherently an identification of which cell the selected symbol table belongs to.

Regarding claim 13:

The rejection of claim 1 is incorporated, and further, Miyadera et al disclose selecting a symbol table as active ("the relocation tables are selected..." in col. 6 lines 42-43. Since the relocation table is selected and will be used, it is inherently the active symbol table.)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 3, 14, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,769,770 to Miyadera et al in view of U.S. Patent 6,275,956 to On et al.

Regarding claim 2:

The rejection of claim 1 is incorporated, and further, Miyadera et al do not disclose a debugger connected to the computer system as set forth in claim 1. On et al disclose in an analogous multi-processor system a debugger for debugging the parallel system ("employing a parallel debugger and its debugging method..." in col. 3 lines 50-51). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the debugging system of On et al with the address relocation system of Miyadera et al, as this would allow a user to test the relocated data using the debugger for the purpose of ensuring proper functionality of the relocated data in Miyadera et al's disclosed system.

Regarding claim 3:

The rejection of claim 2 is incorporated, and further, Miyadera et al do not disclose performing steps each time a debugger transitions from an executing mode to a command mode. On et al disclose in an analogous multi-processor system a debugger as claimed. ("The program is run until it hits the point of the debugging event. At the point of the debugging event is examined information of the program execution..." in col. 5 lines 51-54). Since the program is executing until it hits a debugging event, and data is then examined, this signifies a transition from an executing mode to a debugger (command) mode. It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the debugging system of On et al with the address relocation system of

Miyadera et al, as this would allow a user to test the relocated data using the debugger for the purpose of ensuring proper functionality of the relocated data in Miyadera et al's disclosed system.

Regarding claim 14:

The rejection of claim 13 is incorporated, and further, Miyadera et al do not disclose a debugger using a symbol table which is marked as active. On et al disclose in an analogous multi-processor system a debugger as claimed. ("The program is run until it hits the point of the debugging event. At the point of the debugging event is examined information of the program execution..." in col. 5 lines 51-54). The debugger must be using the symbol table marked as active since it must locate symbol values in order to examine information relating to program execution. It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the debugging method of On et al with the address relocation system of Miyadera et al, as this ensure that the debugger is only checking symbols that have been actively selected and relocated in the system disclosed by Miyadera et al.

Regarding claim 23:

Miyadera et al teach:

- a computer ("an information processing apparatus..." in col. 2 lines 38-39)
- a plurality of symbol tables ("a plurality of relocation tables..." in col. 6 line 39)
- automatic symbol table selection means for automatically selecting at least one of said plurality of symbol tables in said computer for said debugger ("pointers are provided for identifying the relocation tables...the relocation tables are selected...by using the content of

the pointer." in col. 6 lines 39-44. The system automatically selects the corresponding table according to the content of the pointer.)

Miyadera et al do not disclose a debugging apparatus and a debugger connected to the computer system. On et al disclose in an analogous multi-processor system a debugging apparatus for debugging the parallel system ("employing a parallel debugger and its debugging method..." in col. 3 lines 50-51). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the debugging system of On et al with the address relocation system of Miyadera et al, as this would allow a user to test the relocated data using the debugger for the purpose of ensuring proper functionality of the relocated data in Miyadera et al's disclosed system.

Regarding claim 24:

The rejection of claim 23 is incorporated, and further, the limitation regarding a plurality of processing cells is rejected for the reasons set for in connection with claim 7.

8. Claims 6, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,769,770 to Miyadera et al in view of U.S. Patent 5,652,889 to Sites.

Regarding claim 6:

The rejection of claim 5 is incorporated, and further, Miyadera et al do not disclose a program counter. Sites discloses in an analogous memory address relocation system a program counter ("the program counter..." in col. 10 line 55). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the program counter of Sites with the address relocation system of Miyadera et al, as the program counter would be useful in determining what

instruction is currently executing on the processor of the computer system as disclosed by Miyadera et al.

Regarding claim 16:

Miyadera et al teach:

- an apparatus ("an information processing apparatus..." in col. 2 lines 38-39)
- automatically selecting a symbol table in a computer ("the relocation tables are selected...using the content of the pointer." in col. 6 lines 42-44)
- a plurality of symbol tables ("a plurality of relocation tables..." in col. 6 line 39)
- at least one computer readable storage medium ("a scalar processor...makes access to a main storage..." in col. 4 lines 46-47)
- computer readable program code stored on the at least one computer readable storage medium ("the program arrangement in the logical address space..." in col. 4 lines 50-51)
- code for identifying one of the plurality of symbol tables ("pointers...for identifying the relocation tables..." in col. 6 lines 41-42)
- selecting one of the plurality of symbol tables ("the relocation tables are selected...using the content of the pointer." in col. 6 lines 42-44)

Miyadera et al do not disclose a program counter. Sites discloses in an analogous memory address relocation system a program counter ("the program counter..." in col. 10 line 55). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the program counter of Sites with the address relocation system of Miyadera et al, as the program counter would be useful in determining what instruction is currently executing on the processor of the computer system as disclosed by Miyadera et al.

Regarding claim 17:

The rejection of claim 16 is incorporated, and further, Miyadera et al disclose a plurality of symbol tables including symbols stored within an address range ("the content corresponding to each job is written in each of the relocation tables." in col. 6 lines 40-41) and wherein code for identifying whether an address is within an address range for one of the plurality of symbol tables ("the relocation tables are selected...using the content of the pointer." in col. 6 lines 42-44)

9. Claims 8-12 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,769,770 to Miyadera et al in view of U.S. Patent 5,742,828 to Canady et al.

Regarding claim 8:

The rejection of claim 7 is incorporated, and further, Miyadera et al do not disclose a base symbol table and a plurality of secondary symbol tables as claimed in claim 8. Canady et al disclose in an analogous computer system for identifying specific symbol tables a base symbol table and a plurality of secondary symbol tables as claimed. Note Figures 1 and 2 and the corresponding section of the disclosure. It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the symbol table structure of Canady et al in the address relocation system of Miyadera et al, as this would save memory space by utilizing a base symbol table rather than individual symbol tables, wherein the base symbol table can be accessed by the multiple processors in the system disclosed by Miyadera et al.

Regarding claim 9:

The rejection of claim 8 is incorporated, and further, Miyadera et al disclose an address offset ("the real address is obtained by adding the second entry and the lower address..." in col. 3 lines 3-4). However, Miyadera et al do not disclose a plurality of symbol tables contained in a symbol table set, wherein the symbol tables comprise a reference to a base symbol table and a cell identifier. Canady et al disclose a plurality of symbol tables as claimed. Note Figures 1 and 2 and the corresponding section of the disclosure. It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the symbol table organization of Canady et al in the address relocation system of Miyadera et al, as this would ensure that the symbol tables would not overlap and duplicate information.

Regarding claim 10:

The rejection of claim 8 is incorporated, and further, Miyadera et al do not disclose examining a base symbol table before at least one secondary symbol tables. Canady et al disclose examining a base symbol table before examining secondary tables ("searches its global symbol tables...if no match...is found in the global symbol tables...the compiler searches the symbol tables associated with the application libraries..." in col. 6 lines 49-58) It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the examining procedure as stated in Canady et al with the address relocation system of Miyadera et al, as this would ensure that any secondary symbols dependent on the base symbols would not be accessed out of order, ensuring dependency requirements are met.

Regarding claim 11:

The rejection of claim 8 is incorporated, and further, Miyadera et al do not disclose examining a secondary symbol table only if an address pointer is not pointing to a base symbol table. Canady et al disclose examining a secondary symbol table after a pointer is not found in a base symbol table ("searches its global symbol tables...if no match...is found in the global symbol tables...the compiler searches the symbol tables associated with the application libraries..." in col. 6 lines 49-58) It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the examining procedure as stated in Canady et al with the address relocation system of Miyadera et al, as this would ensure that any secondary symbols dependent on the base symbols would not be accessed out of order, ensuring dependency requirements are met.

Regarding claim 12:

The rejection of claim 8 is incorporated, and further, Miyadera et al do not disclose checking a cell identifier as claimed. Canady et al disclose checking a cell identifier within a plurality of symbol tables as claimed. Note Figures 1 and 2 and the corresponding section of the disclosure. It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the cell identifier checking method of Canady et al for the identification of tables in the address relocation system of Miyadera et al, as this would safeguard against relocating symbols that do not need further relocation.

Regarding claim 25:

Miyadera et al teach:

- an apparatus ("an information processing apparatus..." in col. 2 lines 38-39)

- automatically selecting a symbol table in a computer ("pointers are provided for identifying the relocation tables...the relocation tables are selected...by using the content of the pointer." in col. 6 lines 39-44. The system automatically selects the corresponding table according to the content of the pointer.)
- a plurality of processing cells ("a plurality of processors..." in col. 2 line 44)
- at least one computer readable storage medium ("a scalar processor...makes access to a main storage..." in col. 4 lines 46-47)
- computer readable program code stored on the at least one computer readable storage medium ("the program arrangement in the logical address space..." in col. 4 lines 50-51)
- code for selecting one of the plurality of symbol tables and using the symbol table with a processing cell ("the relocation tables are selected...using the content of the pointer." in col. 6 lines 42-44. The symbol table is selected to run on one of the processors of the system.)

Miyadera et al do not disclose a symbol table having a cell identification. Canady et al disclose symbol tables having a cell identification ("searches its global symbol tables for an identifier..." in col. 6 line 41). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the cell identification properties of Canady et al in the address relocation system of Miyadera et al, as this would ensure that only one processor is attempting to relocate objects at any one time in the system disclosed by Miyadera et al.

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,769,770 to Miyadera et al in view of U.S. Patent 5,963,740 to Srivastava et al.

Regarding claim 15:

The rejection of claim 1 is incorporated, and further, Miyadera et al do not disclose an architectural simulator. Srivastava et al disclose in an analogous computer system using relocation tables the use of a computer simulator ("the simulated operation of the computer system is monitored..." in col. 1 lines 54-55) It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the architectural simulator of Srivastava et al with the address relocation system of Miyadera et al, as this would enable a developer to simulate whether the address relocations would optimize running time of a computer program.

11. Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,769,770 to Miyadera et al in view of U.S. Patent 5,652,889 to Sites and further in view of U.S. Patent 5,742,828 to Canady et al.

Regarding claim 18:

The rejection of claim 16 is incorporated, and further, neither Miyadera et al nor Sites disclose determining whether an address falls within a base symbol table. Canady et al disclose determining whether an address falls within a base symbol table. (Note Figures 1 and 2 and the corresponding section of the disclosure). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the symbol table structure of Canady et al in the address relocation system of Miyadera et al, as this would save memory space by utilizing a base symbol table rather than individual symbol tables, wherein the base symbol table can be accessed by the multiple processors in the system disclosed by Miyadera et al.

Regarding claim 19:

The rejection of claim 16 is incorporated, and further, neither Miyadera et al nor Sites disclose determining whether an address falls within an offset symbol table. Canady et al disclose determining whether an address falls within an offset symbol table. (Note Figures 1 and 2 and the corresponding section of the disclosure). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the examining procedure as stated in Canady et al with the address relocation system of Miyadera et al, as this would ensure that only currently used tables are relocated in the system disclosed by Miyadera et al.

Regarding claim 20:

The rejection of claim 19 is incorporated, and further, the limitation regarding a plurality of processing cells is rejected for the reasons set for in connection with claim 7.

Regarding claim 21:

The rejection of claim 20 is incorporated, and further, neither Miyadera et al nor Sites disclose determining whether a cell identifier refers to one of said plurality of processing cells. Canady et al disclose determining whether a cell identifier refers to one of said plurality of processing cells (Note Figures 1 and 2 and the corresponding sections of the disclosure). It would have been obvious to someone of ordinary skill in the art at the time the invention was made to use the cell identifying ability of Canady et al with the address relocation system of Miyadera et al, as this would ensure that relocation is not attempted by multiple processors at the same time in the system disclosed by Miyadera et al.

Regarding claim 22:

The rejection of claim 16 is incorporated, and further, Miyadera et al disclose determining whether a symbol table is enabled for automatic selection ("the relocation tables are selected...using the content of the pointer." in col. 6 lines 42-44. The system must determine whether the table is selectable for the table to be selected in the first place.)

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trent J Roche whose telephone number is (703)305-4627. The examiner can normally be reached on Monday-Friday, 8:30 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Trent J Roche
Examiner
Art Unit 2124

TJR

ANTONY NGUYEN-BA
PRIMARY EXAMINER